Listing of Claims:

Claims 1-56 (cancelled)

Claim 57 (new) A method comprising:

setting a first indicator, the first indicator comprising only a portion of a computer program instruction; and

halting execution of the computer program instruction in response to setting the first indicator.

Claim 58 (new) The method of claim 57, wherein the first indicator comprises one of only a portion of a computer program opcode or only a portion of a computer program micro-operation.

Claim 59 (new) The method of claim 57, wherein the first indicator is one data bit of a computer program opcode.

Claim 60 (new) The method of claim 57, further comprising:

setting a second indicator; and

finishing execution of the computer program instruction in response to setting the second indicator.

Claim 61 (new) The method of claim 60, wherein the second indicator comprises a data bit held in a register.

Claim 62 (new) An apparatus comprising:

a processor; and

a first indicator configurable to halt execution of a computer program instruction by the processor, wherein the first indicator comprises only a portion of the computer program instruction.

Claim 63 (new) The apparatus of claim 62, wherein the first indicator comprises one of only a portion of a computer program opcode or only a portion of a computer program micro-operation.

Claim 64 (new) The apparatus of claim 62, wherein the first indicator is one data bit of a computer program opcode.

Claim 65 (new) The apparatus of claim 62, further comprising:

a second indicator configurable to instruct the processor to finish execution of the computer program instruction.

Claim 66 (new) The apparatus of claim 65, wherein the second indicator comprises a data bit held in a register coupled to the processor.

Claim 67 (new) A system comprising:

a processor to execute a computer program instruction;

a memory coupled to the processor, the memory to store the computer program instruction to be executed by the processor; and

an indicator configurable to control execution of the computer program instruction by the processor, wherein the indicator comprises only a portion of the computer program instruction.

Claim 68 (new) The system of claim 67, wherein the memory comprises Dynamic Random Access Memory (DRAM).

Claim 69 (new) The system of claim 67, wherein the indicator comprises one of only a portion of a computer program opcode or only a portion of a computer program micro-operation.

Claim 70 (new) The system of claim 67, wherein the indicator comprises a data bit of a computer program opcode.

Claim 71 (new) The system of claim 67, further comprising:

another indicator configurable to instruct the processor to finish execution of the computer program instruction.

Claim 72 (new) The system of claim 71, wherein the another indicator comprises a data bit held in a register coupled to the processor.